WHAT IS CLAIMED IS:

1. A semiconductor component comprising:

a semiconductor die comprising a plurality of die contacts;

a plurality of conductors on the die in electrical communication with the die contacts;

a plurality of bumped contacts on the die in electrical communication with the conductors; and

a plurality of test contacts on the die in electrical communication with the conductors;

the test contacts and the bumped contacts configured such that the test contacts can be physically and electrically contacted by contacts of an interconnect without interference from the bumped contacts for applying test signals to the die.

2. The component of claim 1 wherein the test contacts are aligned with the die contacts.

3. The component of claim 1 wherein the test contacts comprise openings in a passivation layer on the die aligned with selected portions of the conductors.

4. The component of claim 1 wherein the test contacts comprise pads on the die in electrical communication with the conductors.

5. A semiconductor component comprising:

a die comprising a plurality of die contacts;

a plurality of conductors on the die in electrical communication with the die contacts;

a plurality of bumped contacts bonded to the conductors;

a plurality of test contacts on the die aligned with the die contacts and comprising selected portions of the conductors;

the test contacts configured for electrical engagement by contacts of a test interconnect to permit testing of the component or the die using the test interconnect.

6. The semiconductor component of claim 5 wherein the test interconnect comprises a probe card and the contacts comprise needle probes, buckle beam probes, spring segment probes or silicon probes.

7. The semiconductor component of claim 5 further comprising a passivation layer on the die and the test contacts comprise a plurality of openings in the passivation layer to the conductors.

8. The semiconductor component of claim 5 wherein the test contacts comprise pads on the selected portions of the conductors.

9. The semiconductor component of claim 5 wherein the component is contained on a wafer comprising a plurality of components.

10. A semiconductor component comprising:

a semiconductor die comprising a face, and a plurality of die contacts on the face;

a plurality of conductors on the face in electrical communication with the die contacts and having first portions and second portions;

an outer passivation layer on the face and on the conductors;

a plurality of first openings in the passivation layer aligned with the first portions of the conductors;

a plurality of bumped contacts located within the first openings and bonded to the first portions of the conductors;

a plurality of test contacts comprising second openings in the outer passivation layer aligned with the second portions of the conductors;

the second openings and the bumped contacts configured to allow electrical access to the second portions for testing the component.

11. The semiconductor component of claim 10 wherein the test contacts comprise a conductive material within the second openings substantially planar to a surface of the outer passivation layer.

12. The semiconductor component of claim 10 wherein the test contacts comprise a conductive material within the second openings which are raised relative to a surface of the outer passivation layer.

13. The semiconductor component of claim 10 wherein the bumped contacts comprise an array of solder balls.

14. The semiconductor component of claim 10 wherein the second openings are aligned with the die contacts.

15. The semiconductor component of claim 10 wherein the conductors have a "fan out" configuration, or a "fan in" configuration.

16. The semiconductor component of claim 10 wherein the test contacts comprise pads on the second portions of the conductors.

17. A semiconductor component comprising:

a semiconductor die comprising a plurality of die contacts and a die passivation layer;

a redistribution circuit on the die comprising:

a plurality of conductors on the die passivation layer in electrical contact with the die contacts and having first portions and second portions;

an outer passivation layer on the die passivation layer and on the conductors;

a plurality of bumped contacts on the die bonded to the first portions of the conductors; and

a plurality of test contacts comprising openings through the outer passivation layer aligned with the second portions of the conductors;

the openings located relative to the bumped contacts such that the second portions of the conductors can be physically and electrically contacted by a plurality of interconnect contacts.

18. The semiconductor component of claim 17 wherein the component comprises a flip chip package.

19. The semiconductor component of claim 17 wherein the bumped contacts comprise an array of solder balls.

20. The semiconductor component of claim 17 wherein the openings are aligned with the die contacts.

21. A method for testing semiconductor components comprising:

providing an interconnect comprising a plurality of interconnect contacts;

providing a component comprising a plurality of bumped contacts and a plurality of test pads in electrical communication with the bumped contacts, the test contacts configured for physical and electrical contact by the interconnect contacts without interference from the bumped contacts;

electrically contacting the test contacts with the interconnect contacts; and

applying test signals through the interconnect contacts and the test contacts to the component.

22. The method of claim 21 wherein the component is contained on a semiconductor wafer comprising a plurality of components.

23. The method of claim 21 wherein the component comprises a semiconductor wafer and the interconnect comprises a probe card.

24. The method of claim 21 wherein the interconnect contacts comprise needle probes comprising generally orthogonal tip portions having a first height greater than a second height of the bumped contacts.

25. A method for testing semiconductor components comprising:

providing the components on a wafer comprising a plurality of semiconductor dice and a plurality of die contacts on the dice;

providing an interconnect comprising a plurality of interconnect contacts configured to electrically contact the die contacts;

forming a plurality of bumped contacts on the wafer in electrical communication with the die contacts, and a

plurality of test pads on the wafer in electrical communication with the bumped contacts, the test contacts configured for physical and electrical contact by the interconnect contacts without interference from the bumped contacts; and

following the forming step, testing the dice by electrically contacting the test contacts with the interconnect contacts and applying test signals through the interconnect contacts to the test contacts.

26. The method of claim 25 further comprising forming the test contacts in alignment with the die contacts and prior to the forming step testing the dice by applying second test signals through the interconnect contacts to the die contacts.

27. The method of claim 25 wherein testing the dice comprises mounting the interconnect and the wafer on a wafer prober and moving the wafer into contact with the interconnect.

28. The method of claim 25 wherein the interconnect comprises a probe card selected from the group consisting of needle probe cards, buckle beam probe cards, spring segment probe cards and silicon probe cards.

29. A method for testing semiconductor components comprising:

providing a component comprising a semiconductor die, a plurality of die contacts, a plurality of conductors in electrical communication with the die contacts, and a plurality of bumped contacts on the conductors;

providing a plurality of test pads on the conductors;

providing an interconnect comprising a plurality of interconnect contacts configured to electrically engage the test pads, the interconnect contacts configured such that the test contacts can be physically and electrically contacted without interference from the bumped contacts;

electrically contacting the test contacts with the interconnect contacts; and

applying test signals through the interconnect contacts and the test contacts to the die.

30. The method of claim 29 wherein test pads are aligned with the die pads.

31. The method of claim 29 wherein the interconnect contacts comprise needle probes comprising generally orthogonal tip portions having a first height greater than a second height of the bumped contacts.

32. The method of claim 29 wherein the interconnect contacts comprise buckle beam probes comprising movable tip portions having a first height greater than a second height of the bumped contacts.

33. The method of claim 29 wherein the interconnect contacts comprise spring segment probes having a first height greater than a second height of the bumped contacts.

34. The method of claim 29 wherein the interconnect contacts comprise silicon probes having a first height greater than a second height of the bumped contacts.

35. A method for testing a semiconductor component comprising:

providing a semiconductor die comprising a plurality of die contacts;

providing a redistribution circuit on the die comprising a plurality of conductors on the die in electrical communication with the die contacts, an outer passivation layer on the die and the conductors, and a plurality of bumped contacts bonded to the conductors;

providing a plurality of test contacts on the die comprising a plurality of openings in the passivation layer to the conductors;

providing an interconnect comprising a plurality of interconnect contacts configured to physically and electrically contact the test contacts without interference from the bumped contacts;

electrically contacting the test contacts with the interconnect contacts; and

applying test signals through the interconnect contacts and the test contacts to the die.

36. The method of claim 35 wherein the test contacts are aligned with the die contacts to permit testing of the component or the die using the interconnect.

37. The method of claim 35 wherein the die is contained on a wafer comprising a plurality of dice.

38. The method of claim 35 wherein electrically contacting the test contacts comprises moving the interconnect towards the component

39. The method of claim 35 wherein the interconnect is mounted to a wafer prober configured to move the interconnect or the die such that the interconnect contacts electrically engage the test contacts.

40. The semiconductor method of claim 35 wherein the component comprises a flip chip package.

41. A system for testing a semiconductor component having bumped contacts comprising:

a plurality of test contacts on the component in electrical communication with the bumped contacts;

an interconnect comprising a plurality of interconnect contacts configured to electrically engage the test contacts without interference from the bumped contacts; and

a testing circuit in electrical communication with the interconnect contacts configured to apply test signals to the component.

42. The system of claim 41 wherein the component comprises a wafer the system further comprises a wafer prober for moving the wafer towards the interconnect for electrically engaging the test contacts.

43. The system of claim 41 wherein the component comprises a singulated package and the system further comprises a test carrier for temporarily packaging the package in electrical communication with the interconnect.

44. A system for testing a semiconductor wafer having bumped contacts comprising:

a wafer prober;

an interconnect on the wafer prober comprising a plurality of interconnect contacts;

a testing circuit in electrical communication with the interconnect contacts configured to generate test signals; and

a redistribution circuit on the wafer comprising a plurality of conductors in electrical communication with the bumped contacts, an outer passivation layer on the wafer, and a plurality of test contacts comprising openings in the passivation layer aligned with selected portions of the conductors, the test contacts and the bumped contacts configured for electrical engagement by the interconnect contacts.

45. The system of claim 44 wherein the interconnect comprises a probe card selected from the group consisting of needle probe cards, buckle beam probe cards, spring segment probe cards and silicon probe cards.

46. The system of claim 44 wherein the test contacts are aligned with die contacts on the wafer.